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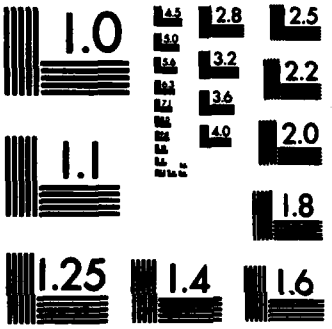

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The final report describes research in hardware synthesis, layout, compaction and area estimation. The most important results involve the wireability analysis for gate arrays, the derivation of Rent's rule, extensions of Hafer's register-transfer synthesis model, and the specification of a data structure to represent hardware design data for use in an expert system.

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Final Report

Alice C. Parker

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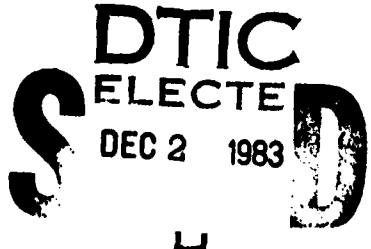

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1. ABSTRACT

This final report describes research in synthesis, layout, compaction and area estimation. The most important results involve the wirability analysis for gate arrays, the derivation of Rent's rule, extensions of Hafer's register-transfer synthesis model, and the specification of a data structure to represent hardware design data for use in an expert system.

2. INTRODUCTION

This final report summarizes research performed in three areas: layout and compaction, synthesis, and area estimation. Most of the research results have been published and will be summarized here. Research results from 1979-1980 while the author was at Carnegie-Mellon University have been published separately as a final report under Grant #DAAG29-79-C-0197. A list of publications and supported personnel follows the research summary.

3. SUMMARY OF RESEARCH RESULTS

In order for higher-level synthesis programs to evaluate design tradeoffs, the programs must have available accurate performance and area estimates. Therefore, in parallel with the research on mathematical modeling of the synthesis process and its relationship to verification, research was also performed on layout and area estimation.

3.1. Synthesis

Synthesis research has involved two extensions of Hafer's model for register-transfer synthesis [4], a method for increasing the efficiency of the synthesis procedure, an examination of the relationship between synthesis and verification (which is ongoing research), and the construction of an expert system for synthesis.

The first extension of Hafer's model involved automating the design of testable hardware [9]. This research showed how to introduce controllability and observability constraints into a synthesis problem in much the same way timing constraints are used. The second extension included interconnections in Hafer's model. This extension is necessary in order to use Hafer's model for verification and is still being researched.

A method for more efficient synthesis using Hafer's model was proposed and tested [2]. This method involves detecting whether a new data path configuration is better than the present configuration without solving the timing part of the optimization procedure, which is linear. It is useful for objective functions which change monotonically as design variations are made.

The Expert Synthesis System research has mostly been involved with the overall system goals and capabilities, and with the detailed specification of the design data structure [5, 6]. Although much of the research so far is preliminary, the design of the data structure is complete, and it has been shown to be useful for some verification tasks.

3.2. Layout and Compaction

Layout and compaction research has focused on metric-free (relative) placement procedure. PLATES, a layout language specifying relative spacings was proposed [11]. PLATES is a symbolic representation scheme for describing layouts that

1. Enables a designer to describe layouts topologically without having to specify sizes, distances, or extents of overlaps of the various regions of semiconductor material.

2. Frees the designer from having to explicitly specify the constraints imposed by the technology. Thus the representation is independent of technology.

3. Allows the designer to compose layout descriptions hierarchically.

The next part of this effort focused on algorithms for generating "correct" and "compact" layouts given a representation of the layout in PLATES. A "correct" layout is one that satisfies all the geometric constraints imposed by the technology. The first phase of this work was a study involving compaction of X and Y directions separately. The results of this work are a collection of algorithms that

1. Take a PLATES description and a set of design rules imposed by the technology and produce a pair of acyclic, directed graphs. g_x and g_y, that represent the constraints that have to be satisfied by the elements of the layout. The nodes of the graphs correspond to the coordinates of the vertical and horizontal edges of the rectangles that comprise the layout, and the edges correspond to the constraints between the nodes. This phase is called the Constraint Generation Phase.

2. Compact the layout (subject to the constraints produced the Constraint Generation Phase) by first finding the critical paths in g_x and g_y and then assigning optimal values to the other nodes. This phase is known as the Constraint Satisfaction Phase.

Thus the result is a correct and compact layout, with the compaction in the X and Y directions done separately. Although this method is not novel, the derivation of the graphs from this layout language is a new approach.

The second phase of this compaction research involved the problem that some rectangles may only be partially ordered in the input specification. We presented this problem in graph-theoretic terms and analyzed its complexity. Thus we proved that optimal compaction of two-dimensional layouts is NP-complete [12].

3.3. Area Estimation

Research on area estimation has involved register-transfer design tradeoffs and routing area for regular layouts (e.g., gate arrays).

The register-transfer area research involved an experiment to determine how register-transfer tradeoffs affect the resultant silicon area and performance of layouts [3]. Six register-transfer level designs, each performing the same function with different register transfer level structure, were implemented using a library of CMOS/SOS standard cells, and an automatic placement and routing program. The consumption of area and the critical path timing were calculated for each design. The results show that register-transfer design variations do produce the expected changes in area and performance at the layout level. However, optimistic timing analysis at the RT level, variations in relative storage timing across technologies, and omission of fanout and path length delays altered the resultant area and timing values from those predicted at the RT level. New unpublished experimental results show that the control area for this experiment varies inversely with data path area and we are continuing research to determine under what circumstances each effect dominates total area.

Wirability analysis for gate arrays and other regular layouts involves estimation of routing area (channel widths). We have derived a stochastic model for estimating the

amount of wiring space (i.e. the dimensions of the routing channels) needed for a master-slice integrated circuit [13]. A master-slice IC is modelled as a NxN lattice of points, with each point representing the intersection of a horizontal and vertical channel. Wires are assumed to follow minimal rectilinear paths and allowed to use as many vias as necessary. Wires at an intersection are classified as belonging to one of six classes. Distributions of the number of each type at a channel intersection are derived. As the dimensions of a channel intersection are functions of the number of wires belonging to each class, expected values of these quantities are derived. Finally, preliminary results on extending the model to allow wires with only a fixed number of vias have been obtained.

[14] presents a model that characterizes the relation between wire length distributions and placement of logic on master slice ICs. In particular, the model provides a firm mathematical basis for the well known empirical relation known as Rent's Rule. It is shown that Rent's Rule is a manifestation of a more fundamental underlying process characterized by a function from which the distribution of wire lengths can be recovered (i.e. Rent's Rule contains all the information about the distribution of wire lengths). Based on this, estimates of average wire lengths are derived. Experimental results are shown in the report.

3.4. Other Publications

Other publications were produced under this grant, primarily as a result of previous grant research. These are [8], [1], [7] and [10].

4. PERSONNEL SUPPORTED

Alice C. Parker was supported as principal investigator 9/80 - 8/83.

Sarma Sastry was supported as a research assistant 11/80 - 8/83.

Fadi Kurdahi and Nohbyung Park were supported 40% as research assistants 6/83 - 8/83.

Louis Hafer was supported as a research assistant 6/81.

References

1. Breuer, M. A. and Parker A. C. Digital System Simulation: Current and Future Trends. Proceedings of the 18th Design Automation Conference, IEEE, June, 1981, pp. 269-275.

2. Dervos, D. and Parker, A. C. A Technique for Automatically Producing Optimized Digital Designs. Proceedings of the Mediterranean Electrotechnical Conference,Athens, IEEE, May, 1983, pp. B2.04.

3. Granacki, J.J. and Parker, A.C. The Effect of Register-Transfer Design Tradeoffs on Chip Area and Performances. Proceedings of the 20th Design Automation Conference, December, 1982, pp. .

4. Hafer, L., and Parker, A. "A Formal Method for the Specification Analysis, and Design of Register-Transfer Level Digital Logic." *IEEE Transactions on Computer-Aided Design CAD-2*, 1 (January 1983).

5. Knapp, D. ,Granacki, J. and Parker, A. C. An Expert Synthesis System. Proceedings of the International Conference on Computer Aided Design(ICCAD), ACM-IEEE, September, 1983, pp. 419-424.

6. Knapp, D. and Parker, A. A Data Structure for VLSI Synthesis and Verification. Digital Integrated Systems Center, Dept. of EE-Systems, University of Southern California, October, 1983.

7. Nagle, A. and Parker, A. Algorithms for Multiple-Criterion Design of Microprogrammed Control Hardware. Design Automation Conference Proceedings no. 18, ACM SIGDA, IEEE Computer Society-DATC, June, 1981, pp. 486-493.

8. Nagle, A., Cloutier, R., and Parker, A. "Synthesis of Hardware for the Control of Digital Systems." *IEEE Transactions on Computer-Aided Design CAD-1*, 4 (1982), 201-212.

9. Parker, A. and Hafer, L. Automating the Design of Testable Hardware. Proceedings VLSI 81, 1981, pp. 357-363.

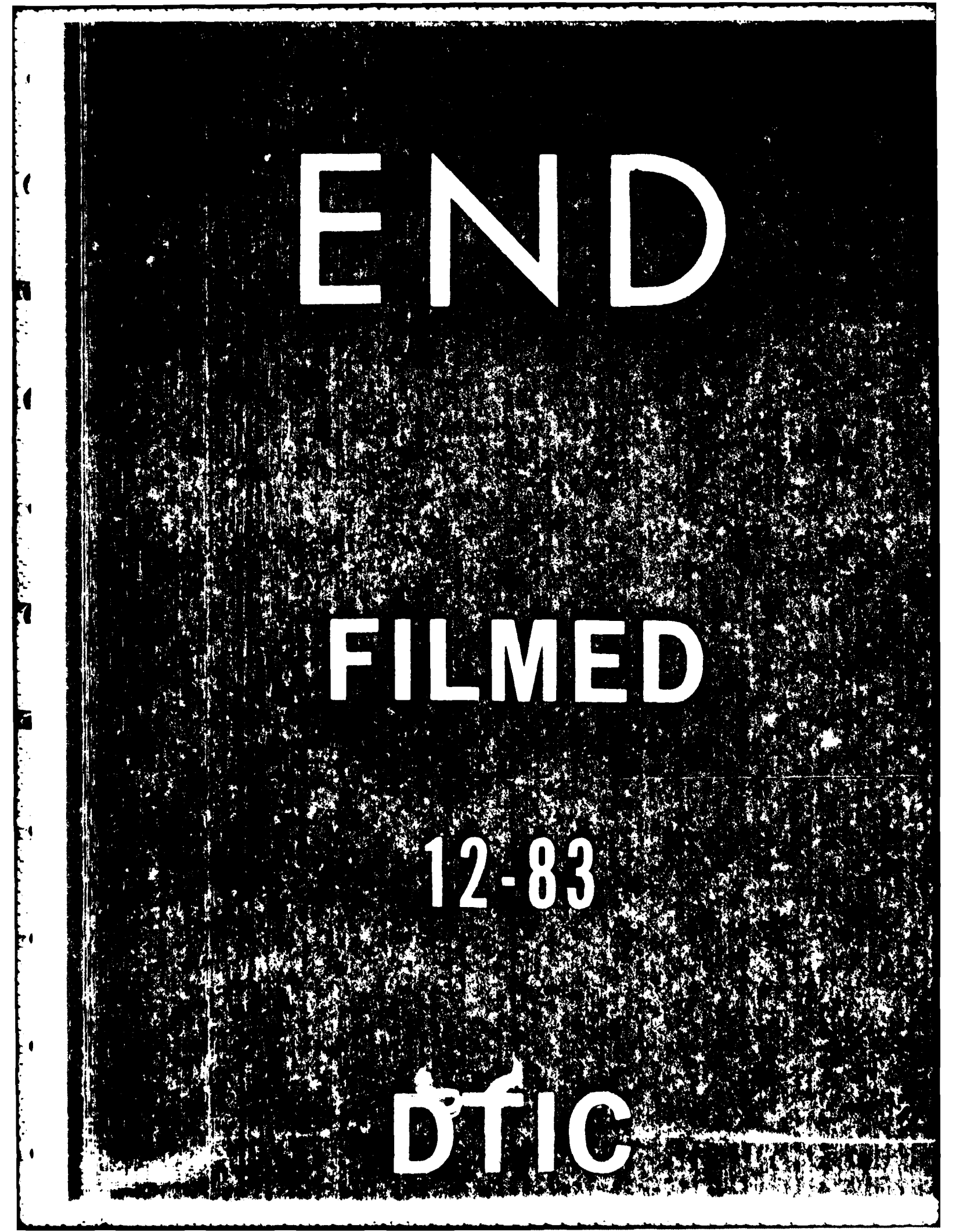
10. Parker, A.C. and Altman, A. System Simulation: A Mixed-Level Approach. Submitted to IEEE Transactions on Computer-Aided Design, 1982

11. Sastry, S. and Klein, S. Plates: A Metric-Free VLSI Layout Language. Proceedings,Conference on Advanced Research in VLSI, MIT, January, 1982, pp. 165-174.

12. Sastry, S. and Parker, A. The Complexity of Two-Dimensional Compaction of VLSI Layouts. Proceedings of the 1982 IEEE International Conference on Circuits and Computers, IEEE, September, 1982, pp. 402-406.

13. Sastry, S. Wiring Space Estimation of Master Slice IC's. Digital Integrated Systems Center, Dept. of EE-Systems, University of Southern California, June, 1983.

14. Sastry, S. On the Relation between Wire Length Distributions and Placement of Logic on Master Slice ICs. Digital Integrated Systems Center, Dept. of EE-Systems, University of Southern California, October, 1983.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